METHOD OF IMPLEMENTATION - DRIVER JITTER

Abstract

This test checks the jitter from the driver using athe WAVECREST SIA 3000. This test is defined for a single lane and must be repeated for each lane of the DUT.

Coverage:

V2c06-007#14

Topology

(1X driver port) = PortPhysical1: Test fixture=PC1X_sma_P1, width=1X

(4X driver port) = PortPhysical1: Test fixture=PC4X_sma_P2, width=4X

(12X driver port) = PortPhysical1: Test fixture=PC1X_sma_P3, width=12X

Qualifier

None

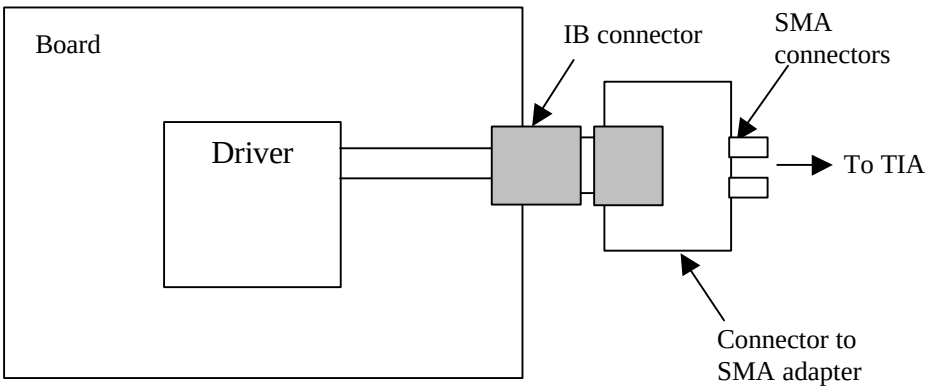
Notes

1. TJ measured at 10^{-12} BER
2. The assumption is that there will be a test point at the cable connector. The TJ and DJ numbers at the cable connector may be different than those listed in Table 15 for the pins of the SERDES.
3. It is assumed that the SERDES can generate continuous TS1 or a pattern generator can be used as an input into the SERDES.
4. Required instruments: SIA 3000 with A32 channel card option.
5. Blocking caps or Wavecrest CML interface module may be used at the input to the SIA 3000.

Dev Notes

Author: Wavecrest, 9/19/02

This test may require an adapter from the Infiniband connector to the test instrument. The drawing below shows a typical test setup



ALGORITHM

Assertions

V2c06-007#14 (Jitter for Driver)

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Initialization

1. Send continuous Bit Pattern (TS1). This test is written around TS1 (pattern length 320) as a test pattern. However, the procedure can be extended to other compliance jitter patterns.

2. Connect SMA differential output from IB driver to input channel of SIA 3000. This may require using a cable connector adapter to SMA adapter and a CML interface module. For example a 1X connector would be converted from HSSDC2 to SMA.

Tester Procedure

1. In VISI DataCom choose the tool Known Pattern with Marker or Random Data with Bitclock. Known Pattern with Marker requires a repeating pattern and Random Data with Bitclock requires a Bit Clock and any type of Data stream.
2. Input corner frequency of 1500 kHz (Bit Rate/1667) (for Known Pattern with Marker only).
3. Select the pattern used for the test TS1 under load pattern.
4. Verify voltage levels are within driver limits of 1.6 to 1.0 V_{pp} by pressing  .
5. Click on  to measure Jitter on SIA 3000
6. Verify DJ ≤ 0.17 UI (this may change depending on the jitter budget along the link)
7. Verify TJ ≤ 0.35 UI

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